High Performance Fully-Depleted Tri-Gate CMOS Transistors

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***Abstract*—Fully-depleted (FD) tri-gate CMOS transistors with 60 nm physical gate lengths on SOI substrates have been fabricated. These devices consist of a top and two side gates on an insulating layer. The transistors show near-ideal subthreshold gradient and excellent DIBL behavior, and have drive current characteristics greater than any non-planar devices reported so far, for correctly-targeted threshold voltages. The tri-gate devices also demonstrate full depletion at silicon body dimensions approximately 1.5–2 times greater than either single gate SOI or non-planar double-gate SOI for similar gate lengths, indicating that these devices are easier to fabricate using the conventional fabrication tools. Comparing tri-gate transistors to conventional bulk CMOS device at the same technology node, these non-planar devices are found to be competitive with similarly-sized bulk CMOS transistors. Furthermore, three–dimensional (3-D) simulations of tri-gate transistors with transistor gate lengths down to 30 nm show that the 30 nm tri-gate device remains fully depleted, with near-ideal subthreshold swing and excellent short channel characteristics, suggesting that the tri-gate transistor could pose a viable alternative to bulk transistors in the near future.**

***Index Terms*—CMOSFET logic devices, CMOSFETs, MOS devices, MOSFET logic devices, MOSFETs.**

I. Introduction

ONE of the challenges facing continued scaling of fully-depleted (FD) SOI transistor is the scaling of the dimensions of the active silicon channel region. In the case of single-gate FDSOI devices, the silicon body thickness (T_{Si}) needs to be about a third to a half of the electrical gate length in order to maintain full substrate depletion under gate control ([1], [2] – see Fig. 1). Scaling this device to 30 nm gate length dimensions, for example, requires a 3-σ thickness uniformity of 1 nm on a silicon film thickness of 10 nm, which is presently hard to achieve. For non-planar double-gate FinFET devices, the transistor structure most often considered for future scaled transistors [3], the thickness requirement for the silicon between the two gates (W_{Si}- see Fig. 1) is relaxed to approximately the electrical gate length, or two-thirds the physical gate length since each gate controls half the body thickness [4]. However, since W_{Si} is smaller than the physical gate length, the most critical lithography step in printing the double-gate transistor becomes the patterning of the Fin, rather than the physical gate length patterning [4]. More importantly, the tall vertical structure of the FinFET device presents significant challenges to device fabrication, since the transistor is fabricated vertical to the wafer plane on processing tools developed largely for planar horizontal devices.

Recently, non-planar tri-gate transistors were simulated [5] and they have also been reported to show fully depleted behavior at thickness dimensions greater than those of the single-gate FD SOI and double-gate FinFET [6].

In this letter, we report on the experimental results of tri-gate CMOS transistors with 60 nm physical gate lengths (L_g). $L_g = 60$ nm was chosen because the technology is mature enough to make a valid comparison with bulk devices—at gate lengths significantly shorter than 60 nm, research devices are unoptimized, and it becomes difficult to compare the benefits offered by various transistor architectures. We find that these devices show the highest ever reported performance for non-planar MOS devices for both n- and p-channel transistors for scaled threshold voltages (V_t). We find also that tri-gates are competitive with a similarly-scaled, aggressive bulk CMOS technology at the same technology node. We further present three-dimensional (3-D) simulations of tri-gate transistor structures that show fully depleted behavior at gate lengths of 30 nm. These devices thus show excellent potential as candidates for future scaled CMOS technologies.

II. Device Fabrication and Measurement

Fig. 1(a)–(c) shows schematics of the different types of FD transistor. Fig. 1(d) shows a TEM cross-section through the silicon body of a typical tri-gate transistor. The devices were fabricated as follows: the fin bodies were first fabricated by treating the body in a similar manner to polysilicon, using aggressive gate lithography techniques to get fin widths equal to gate lengths. The fins were then doped to obtain acceptable V_t using conventional boron (for nMOS) or arsenic (for pMOS) implants. No halo implants were used for setting V_t, nor were there any angled implants used anywhere in the process. This is in contrast to double-gate [7], and it is possible since the tri-gate very much resembles the bulk transistor from the processing point-of-view. The gate stack included polysilicon gates, and a conventional physical oxide thickness of 15 Å. Raised source/drains were used to reduce parasitic resistances [2]. Fig. 2 shows the I_d–V_g characteristics of an NMOS transistor whose TEM is shown in Fig. 1(d), while Fig. 3 shows the I_d–V_d characteristics of the same device. The transistor has physical

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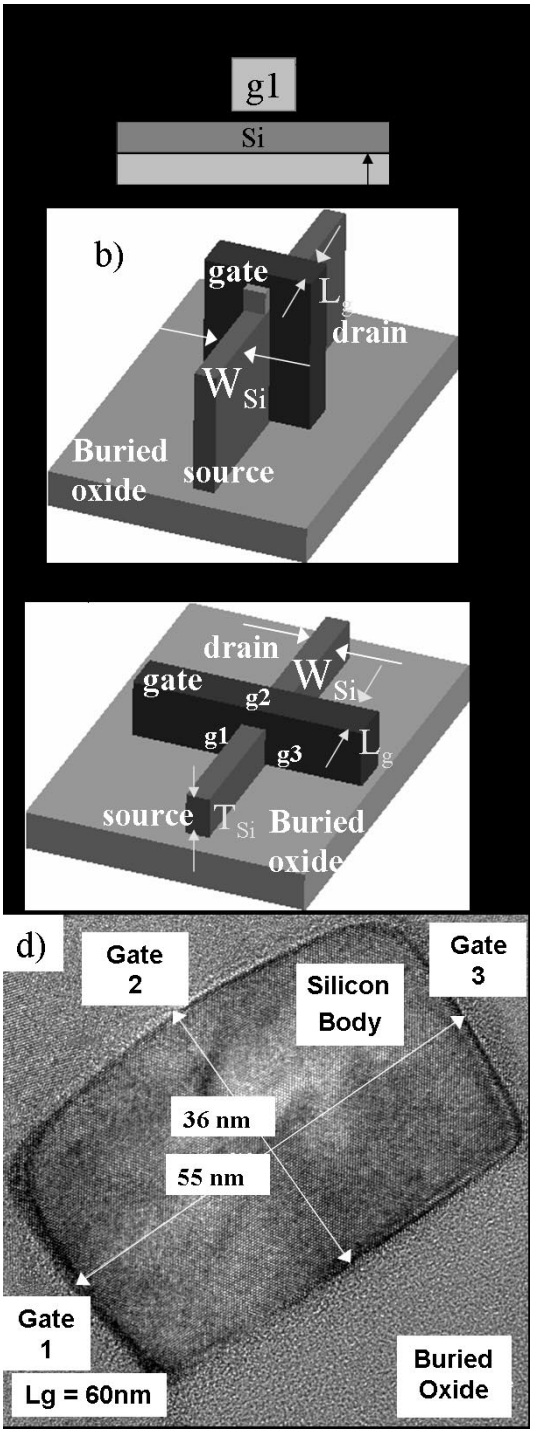

Fig. 1. Illustration of (a) single-gate, (b) double-gate, and (c) tri-gate transistor structures. (d) TEM cross section of the silicon body of the tri-gate NMOS device of Fig. 2.

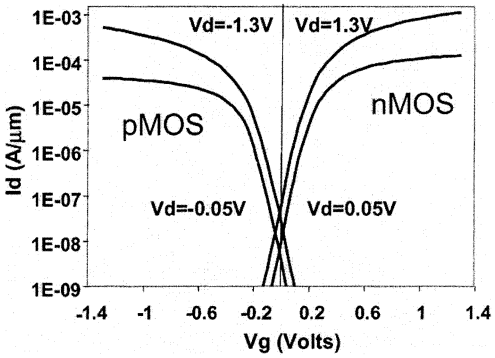

Fig. 2. I_d–V_g characteristics of 60 nm gate length NMOS and PMOS transistors. The current I_d is normalized to the width (Z) in all cases, where $Z = 2 * T_{\rm Si} + W_{\rm Si}$.

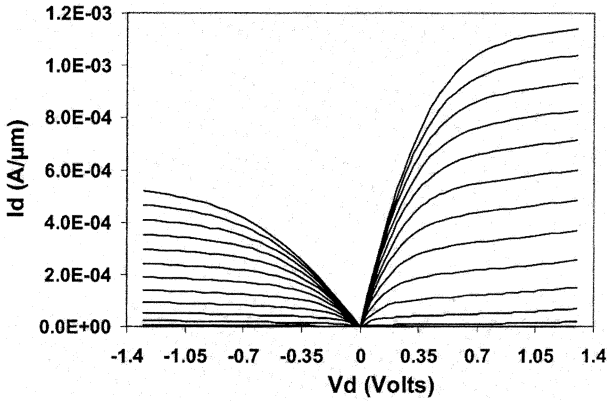

Fig. 3. I_d–V_d characteristics of the 60 nm N- and P-MOS devices of Fig. 2. The gate voltage was ramped to 1.3 V in increments of 0.1 V.

$L_g = 60$ nm, a height $T_{\rm Si} = 36$ nm, and a width $W_{\rm Si} = 55$ nm. This transistor exhibits excellent short channel effects with drain induced barrier lowering $(DIBL) = 41$ mV/V (defined as $\{V_g@V_d = 1.3\ \text{V} - V_g@V_d = 0.05\ \text{V}\}/(1.3 - 0.05)$ where V_g is taken at $I_d = 0.1\mu\text{A}/\mu\text{m}$) and subthreshold slope $(S/S) = 68$ mV/dec.. The complete absence of any kink effect indicates that the device is fully depleted. The transistor also has a drive current (at $V_g = V_d = 1.3$ V) equal to 1.14 mA/μm, and an off-current (at $V_d = 1.3$ V) of 70 nA/μm. The width (Z) in all cases is taken to be $Z = (2 * T_{\rm Si} + W_{\rm Si})$, representing the top and the two sides of the tri-gate device. This drive current value is the highest reported for non-planar n-channel silicon devices with scaled threshold voltage (other devices have higher $I_{\rm dsat}$ – e.g., [7] but the $I_{\rm off}$ is many orders of magnitude higher). Fig. 2 also shows the I_d–V_g characteristics of the $L_g = 60$ nm tri-gate PMOS device, which has $I_{\rm on} = 521\ \mu\text{A}/\mu\text{m}$ and $I_{\rm off} = 24$ nA/μm at $V_{\rm cc} = 1.3$ V, as well as $DIBL = 48$ mV/V and $S/S = 69.5$ mV/dec.. These drive current values are also the highest reported for non-planar scaled V_t p-channel silicon devices.

From Fig. 1(d), it can be seen that the silicon height $T_{\rm Si}$ ($\sim$ 36 nm) for this tri-gate device is twice as large as that required for full depletion in single-gate SOI devices at this gate length dimension [2]. The width of the silicon body ($\sim$ 55 nm) is also approximately 50% greater than that required for full depletion in double-gate SOI transistors [4]. Thus, the tri-gate devices offer relaxed constraints in body dimensions over other FD transistor options (note that gate-all-around (GAA) [8] or wrap-around (WW) [9] gate devices are not considered here, due to the as-yet unresolved manufacturing difficulty of aligning the bottom gate without high overlap capacitance issues.)

The drive currents for n- and p-MOS tri-gates compare very favorably to bulk CMOS—for a similarly scaled bulk technology with an identical oxide thickness, the $I_{\rm on}$ values recorded are 1.3 and 0.66 mA/μm for N- and P-MOS respectively with $I_{\rm off} = 100$ nA/μm, at 1.4 V [10]. This is close

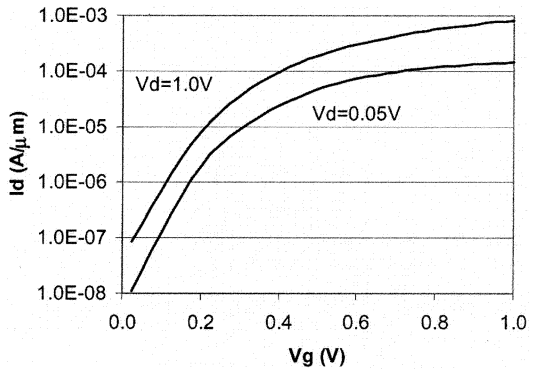

Fig. 4. I_d–V_g characteristics of a simulated NMOS tri-gate transistor, with $L_g = W_{\rm Si} = T_{\rm Si} = 30$ nm, showing subthreshold gradients of 73 mV/decade, and DIBL of 62 mV/V.

to the 1.14 and 0.52 mA/μm current values obtained for the tri-gates (Fig. 2), with a lower supply voltage (1.3 V), and a lower $I_{\rm off}$ ($\sim$ 70 nA/μm).

In order to study the scalability of these devices to smaller gate lengths, 3-D simulations were performed on tri-gate devices, using DESSIS [11]. This simulation extends the work of Leobandung *et al.* [9], taking it down to $L_G = T_{\rm Si} = W_{\rm Si} = 30$ nm. Similarly to Leobandung *et al.*, the proximity of the three gates in the tri-gate device was found to play an important role in controlling current conduction in the body of the device, in contrast to the case of the planar device, where only the top surface is inverted. Fig. 4 shows the simulated I_d-V_g characteristics of the 30 nm device. It can be seen that the device shows near-ideal FD device performance with good DIBL and a steep subthreshold gradient. The simulations also show that the edge device turns on slightly before the bulk of the transistor. Since the edge is a significant proportion of the device width, the "hump" in the log I_d-V_g characteristics sometimes seen in narrow bulk devices is not seen in these tri-gate transistors.

These results suggest not only that the tri-gate concept is scalable to future CMOS technology generations, but, given that the subthreshold gradient of bulk devices continues to degrade with shrinking gate length, the tri-gate transistor is a good candidate to replace bulk transistors in the near future.

III. Summary

FD tri-gate CMOS transistors with gate lengths of 60 nm have been fabricated and compared to well-optimized bulk CMOS transistors at these dimensions. The tri-gate NMOS device has a subthreshold slope $(S/S) = 68$ mV/decade, $DIBL = 41$ mV/V, $I_{\rm on} = 1.14$ mA/μm and $I_{\rm off} = 70$ nA/μm at $V_{\rm cc} = 1.3$ V. The PMOS device shows $S/S = 69.5$ mV/decade, $DIBL = 48$ mV/V, $I_{\rm on} = 520$ μA/μm and $I_{\rm off} = 24$ nA/μm at $Vcc = 1.3$ V. To our knowledge, this is the highest performing non-planar CMOS devices with correctly targeted threshold voltages, and they compare well with optimized production-like bulk CMOS transistors with similar dimensions and processing.

The tri-gate devices show full depletion for much more relaxed silicon body dimensions than those required for single-gate or double-gate FD transistors, with full depletion achieved for a silicon body thickness ($T_{\rm Si} - 36$ nm) approximately double that required for single-gate, and a body width ($W_{\rm Si} - 55$ nm) approximately 1.5 times that required for double-gate SOI transistors at $L_g = 60$ nm. Three–dimensional simulations of the tri-gate transistor with $L_g = T_{\rm Si} = W_{\rm Si} = 30$ nm show that the tri-gate device maintains full depletion at these dimensions, and exhibit excellent short channel performance, and suggest that this transistor design could supplant bulk CMOS transistors in the near future.

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